AF

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Before the Board of Patent Appeals and Interferences

Applicant	:	Aaron Reel Bouillett
Application No.:		10/511,562
Filed	:	October 15, 2004
For	:	EQUALIZER STATUS MONITOR
Examiner	:	Leon Viet Q Nguyen
Art Unit	:	2611

APPEAL BRIEF

Mail Stop: Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

May It Please The Honorable Board:

Applicant appeals from the Office Action dated April 20, 2007, in which claims 1-18 of the above-identified application stand rejected two times.

Applicant waives an Oral Hearing for this appeal.

Please charge the $500.00 fee for filing this Brief to Deposit Account No. 07-0832.

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I. REAL PARTY IN INTEREST

The real party in interest of Application No. 10/428,973 is:

THOMSON LICENSING
46, Quai A. Le Gallo
F-92100 Boulogne-Billancourt
France.

II. RELATED APPEALS AND INTERFERENCES

There are no related Appeals or Interferences.

III. STATUS OF THE CLAIMS

Claims 19-23 have been canceled.

Claims 1-18 and 24-26 are pending in this application.

Claims 1-18 and 24-26 have been rejected.

The rejection of claims 1-18 and 24-26 are appealed.

IV. STATUS OF AMENDMENTS

In response to the Office Action dated April 20, 2007, Applicant's representative filed a Notice of Appeal on July 18, 2007.

This appeal is directed to the claims as they stood at the time of the Office Action of April 20, 2007, which are shown in the Claims Appendix of this Brief.

V. SUMMARY OF CLAIMED SUBJECT MATTER

There are three independent claims pending in the application: 1, 12 and 24. As noted in the background of Applicant's specification, a receiver uses an adaptive equalizer to process a received signal in order to compensate for the effects of changing conditions and disturbances on the signal transmission channel. (Applicant's specification, p. 2, lns. 4-9.) However, an adaptive equalizer has the potential to diverge, or adapt, to an invalid state and, as such, negatively impact receiver performance. (Applicant's specification, p. 5, lns. 11-15.)

In this regard, Applicant's inventive concept tests a sliced version of the equalizer output signal to determine equalizer convergence (or divergence). For example, if the transmitted signal is an 8-level Vestigial SideBand (VSB) signal, each transmitted symbol is taken from the following symbol constellation: {7,5,3,1,-1,-3,-5,-7}. (Applicant's specification, p. 7, lns. 10-14.) A slicer "slices" the equalizer output signal to the closest one of these eight symbols. Applicant's test is applied to this sliced signal. One example of a test is as follows: 400,000 sliced symbols are observed, if every one of the eight symbols of the constellation occurs at least once, then the equalizer is deemed to have converged. (Applicant's specification, p. 8, lns. 11-18.)

In view of the above, Applicant's independent claim 1 is directed to an apparatus comprising a nearest element decision device (e.g., slicer 29 of FIG. 3) and a monitoring circuit (e.g., microprocessor 31 of FIG. 3) for receiving the decision device output signal and applying a test criterion to data (e.g., sliced symbols) contained in the decision device output signal so as to determine equalizer convergence. (Applicant's specification, p. 8, lns. 5-17.)

Applicant's independent claim 12 is similar to Applicant's independent claim 1, except that claim 12 is narrower and includes additional requirements such as an adaptive channel equalizer and that the received signal be a Vestigial SideBand (VSB) signal. (Applicant's specification, p. 7, lns. 10-14.)

Finally, Applicant's independent claim 24 is directed to a method for use in determining equalizer convergence by first slicing the equalizer output signal (e.g., slicer 29 of FIG. 3) to provide a sequence of symbols and then testing a plurality of symbols of the sequence to determine equalizer convergence (e.g., elements 31 and 35 of FIG. 3). (Applicant's specification, p. 8, lns. 5-18.)

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

There are four grounds of rejection to be reviewed on Appeal.

(1) Whether claims 25-26, fail to comply with the written description requirement under 35 U.S.C. § 112, first paragraph.

(2) Whether claims 1-7, 10-12, 15-18 and 24 are unpatentable under 35 U.S.C. § 103(a) over U.S. Patent No. 5,781,463 issued July 14, 1998 to Ogawa et al. (*Ogawa).*

(3) Whether dependent claims 8 and 13 are unpatentable under 35 U.S.C. § 103(a) over *Ogawa* in view of U.S. Patent No. 6,515,713 issued February 4, 2003 to Nam.

(4) Whether dependent claims 9 and 14 are unpatentable under 35 U.S.C. § 103(a) over *Ogawa* in view of U.S. Patent No. 4,697,265 issued September 29, 1987 to Nozue.

VII. ARGUMENT

Rejection of Claims 25 and 26 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement.

CLAIMS 25 and 26

Applicant's claims 25 and 26 pass muster under 35 U.S.C. § 112, first paragraph.

The Examiner has rejected claim 25 because, according to the Examiner, the claim requirements of a constellation comprising an alphabet of N symbols and determining if at least M of the N symbols are represented in the plurality of symbols was not disclosed in the original disclosure. Respectfully, the Examiner is wrong.

First, the requirement in claim 25 of a constellation comprising an alphabet of N symbols is clearly supported in Applicant's specification. Page 7, lns. 9-11, of Applicant's specification clearly states:

> [f]or example, if the permissible transmitted symbol values are −1 and +1, the slicer will only output those values.

Also, page 7, lns. 12-14, of Applicant's specification clearly states:

> [s]imilarly, in the illustrated embodiment of an 8-VSB signal, the permissible symbol values are {7,5,3,1,-1,-3,-5,-7}.

Thus, two examples are clearly described in Applicant's specification – a constellation comprising an alphabet of 2 symbols and a constellation comprising an alphabet of 8 symbols. The mere fact that Applicant has chosen to use algebraic notation in claim 25 does not change the facts. There is clear support in Applicant's specification for alphabets having N symbols, $N>1$. Further, one skilled in the art of communications systems would clearly understand the simple algebraic notation shown in claim 25.

Second, the requirement in claim 25 of determining if at least M of the N symbols are represented in the plurality of symbols is clearly supported in Applicant's specification. Page 8, lns. 15-18, of Applicant's specification clearly states (emphasis added):

> [d]epending on the characteristics of the transmitted signal, the criterion can be modified to require a larger number of each

> possible symbol, or only some fraction of all possible symbol values.

Thus, Applicant's claimed requirement of determining if at least M of the N symbols are represented in the plurality of symbols is clearly supported in Applicant's specification.

Turning now to Applicant's claim 26, the Examiner has rejected claim 26 because, according to the Examiner, the claim requirement that M can be equal to N was not disclosed in the original disclosure. Again, the Examiner is wrong.

The requirement in claim 26 that M can be equal to N is clearly supported in Applicant's specification. Page 8, lns. 11-13, of Applicant's specification clearly states (emphasis added):

> [t]hat is, every one of the permissible symbol values ({7,5,3,1,-1,-3,-5,-7}) must occur at least once in the sample of 400,000 symbols gathered..

In this example, the alphabet of symbols is an 8-level VSB constellation, i.e., $N = 8$. Further, every one of the eight symbols must occur at least once, i.e., $M = N$. As a result, Applicant's claimed requirement that M can be equal to N is clearly supported in Applicant's specification.

In view of the above, Applicant's claims 25 and 26 pass muster under 35 U.S.C. § 112, first paragraph.

Rejection of Claims 1-7, 10-12, 15-18 and 24 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,781,463 (*Ogawa*)

CLAIMS 1-7, 10-12, 15-18 and 24

The Examiner's rejection of claims 1-7, 10-12, 15-18 and 24 under 35 U.S.C. § 103(a) as being unpatentable over *Ogawa* cannot stand for the simple reason that the Examiner's suggested modification to *Ogawa* to yield Applicant's claimed invention is untenable.

CLAIMS 1-7 and 10 ARE PATENTABLE

As described below, the Examiner's argument has two parts: I and II. All of which fail.

Part I of the Examiner's argument

The Examiner asserts with respect to Applicant's claim 1 that *Ogawa* discloses an apparatus comprising:

> an equalizer output signal (the output from 1 and 2 [of FIG. 8 of *Ogawa*];
> a monitoring circuit (6, 31, and 32 in fig. 8 [of *Ogawa*]), the monitoring circuit receiving an output signal (fig. 8 [of *Ogawa*], the output of 30) and applying a test criterion to data contained in the decision device output signal so as to determine equalizer convergence (col. 15, line 58-col. 17 line 3, test criterion being a [sic] the response to a logic "0"or "1").
>
> Office Action dated April 20, 2007, p. 3.

Part II of the Examiner's argument

The Examiner then states that the embodiment of FIG. 8 does not show Applicant's claimed nearest element decision device. In this regard, the Examiner then points to FIG. 3 of *Ogawa* for showing a nearest element decision device (4A) for receiving the equalizer output signal and creating a decision device output signal containing permissible symbol values of a symbol constellation used in transmission of a signal to the apparatus.

From this, the Examiner asserts that it would be obvious to combine the embodiments as a whole to incorporate the decision device of the embodiment shown in FIG 3 of *Ogawa* into the apparatus of the embodiment shown in FIG. 8 of *Ogawa*. As motivation, the Examiner asserts that

> [t]he motivation to combine the two embodiments would be to discriminate to which one of a numerical region that is defined to have a normal code value free from any modulation due to disturbance as a central value (col. 10, lines 42-46 [*Ogawa*])..
>
> Office Action dated April 20, 2007, p. 4.

Response to Part I of the Examiner's argument

With regard to *Part I of the Examiner's argument*, the Examiner is wrong. In particular, the Examiner glosses over the requirements of Applicant's claim 1. In point of fact, Applicant's claim 1 requires:

> an equalizer output signal;
> a nearest element decision device, the nearest element decision device receiving the equalizer output signal and creating a

decision device output signal containing permissible symbol values of a symbol constellation used in transmission of a signal to the apparatus; and

a monitoring circuit, the monitoring circuit receiving the decision device output signal and applying a test criterion to data contained in the decision device output signal so as to determine equalizer convergence.

Thus, as required by Applicant's claim 1, the monitoring circuit must receive and apply a test criterion **to a decision device output signal containing permissible symbol values of a symbol constellation**. The Examiner's citation to elements 6, 32 and 31 of FIG. 8 of *Ogawa* does not perform this function. In particular, counter 31 in FIG. 8 of *Ogawa* counts the size of the error. (*Ogawa*, col. 16, lns. 41-57.) As such, the Examiner's assertion that FIG. 8 already shows Applicant's claimed monitoring circuit is wrong.

Nor does the Examiner's asserted modification to FIG. 8 (described below) rectify this problem since nowhere does *Ogawa* describe or suggest Applicant's claimed monitoring circuit. For example, the arrangement in FIG. 8 of *Ogawa* with respect to element 6 and element 5 does not describe, or suggest, Applicant's claimed monitoring circuit. In particular, element 6 of FIG. 8 of *Ogawa* either outputs an error value or a predetermined value. (*Ogawa*, col. 12, lns. 8-6.) Thus, element 6 does not apply a test criterion as claimed by Applicant. As such, even if one performs the Examiner's substitution (described below) – there is still no description or suggestion in *Ogawa* of a monitoring circuit as claimed by Applicant.

In view of the above, even before one gets to *Part II of the Examiner's argument*, it can be seen that Applicant's claim 1 is patentable.

Response to Part II of the Examiner's argument

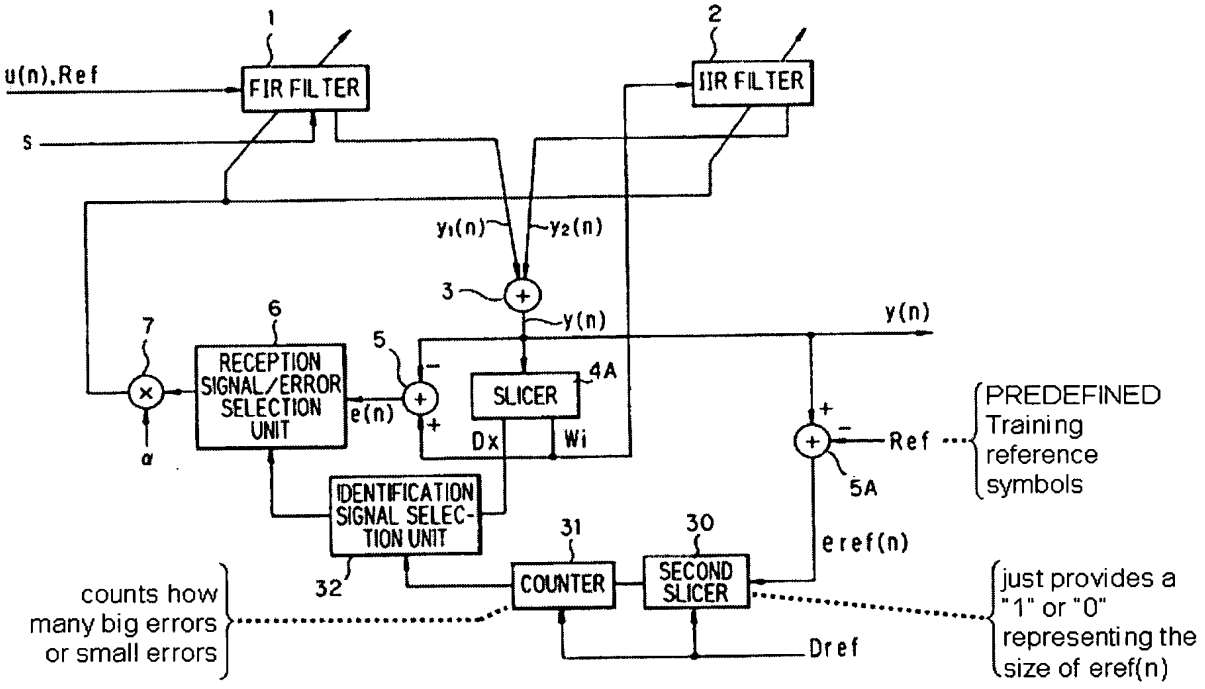
As Applicant's understand the Examiner's position, one skilled in the art would combine the embodiments shown in FIG. 3 of *Ogawa* with FIG. 8 of *Ogawa* to yield Applicant's claimed invention. In particular, the Examiner points to the nearest element decision device, 4A in FIG. 3 of *Ogawa*, and that one skilled in the art would combine it with the embodiment shown in FIG. 8 of *Ogawa*. This argument fails for anyone of a number of reasons.

First, it should be noted that the embodiment shown in FIG. 8 of *Ogawa* already includes the embodiment shown in FIG. 3 of *Ogawa*. Indeed, *Ogawa* states that the "digital

filter of this embodiment [FIG. 8] has substantially the same arrangement as that of the digital filter of the first embodiment shown in FIG. 3". *Ogawa*, col. 15, ln. 66 to col. 16, ln. 1, emphasis added. In other words, combining the embodiments of FIGs. 3 and 8 of *Ogawa* does nothing. As already noted above, the embodiment shown in FIG. 8 of *Ogawa* does not describe, or suggest, Applicant's claimed arrangement.

Second, if the Examiner is stating that it would be obvious to further replace slicer 30 of FIG. 8 of *Ogawa* with slicer 4A of FIG. 3 of *Ogawa* – this is simply wrong. An annotated form of FIG. 8 of *Ogawa* is shown below.

FIG. 8



It should be noted that a training signal is used in the embodiment of FIG. 8 of *Ogawa*. In other words, the receiver already knows what symbols were transmitted. In particular, element 5A of FIG. 8 of *Ogawa* compares the received version of the training signal to the predefined reference training signal. (*Ogawa*, p. 16, lns. 1-4.) Thus, there is not only no reason to replace second slicer 30 with slicer 4A in FIG. 8 of *Ogawa* – it also, respectfully, just makes no sense since the receiver already knows what symbols were transmitted.

As described in *Ogawa*, second slicer 30 provides a logical "1" or "0" which represents a size of the error signal *eref(n)*. For example if the value of *eref(n)* is less than a predetermined value, then second slicer 30 provides a logical "1", otherwise, slicer 30 provides a logical "0". (*Ogawa*, col. 16, lns. 42-51.) Counter 31 counts the types of errors. (*Ogawa*, col. 16, lns. 52-57.) As noted earlier, this arrangement shown in FIG. 8 of *Ogawa* does not show or suggest the requirements of Applicant's claim 1, which require testing the sliced symbols.

Finally, the Examiner's cited motivation for modifying FIG. 8 of *Ogawa* is irrelevant for the same reasons as noted above. First, the embodiment of FIG. 8 of *Ogawa* already includes a slicer 4A. Second, if the Examiner means to replace slicer 30 with slicer 4A in FIG. 8 of *Ogawa*, then the Examiner's stated motivation is simply wrong given the use of a training signal in FIG. 8 of *Ogawa*.

In view of the above, Applicant's claim 1, and, therefore, dependant claims 2-8 are patentable over *Ogawa*.

CLAIMS 12 and 15-18 ARE PATENTABLE

Similar comments apply to Applicant's independent claim 12. As such, Applicant's claim 12 and dependent claims 15-18 stand or fall with Applicant's independent claim 1.

CLAIM 24 IS PATENTABLE

Similar comments apply to Applicant's independent claim 24. As such, Applicant's claim 24 stands or falls with Applicant's independent claim 1.

Rejection of Dependent Claims 8 and 13 under 35 U.S.C. § 103(a) as being unpatentable over *Ogawa* in view of U.S. Patent No. 6,515,713 issued February 4, 2003 to Nam

DEPENDENT CLAIMS 8 and 13

If the rejection of independents claims 1 and 12 fall, then dependent claims 8 and 13 are patentable. As such, the rejection of dependent claims 8 and 13 stands or falls with Applicant's independent claim 1.

Rejection of Dependent Claims 9 and 14 under 35 U.S.C. § 103(a) as being unpatentable over *Ogawa* in view of U.S. Patent No. 4,697,265 issued September 29, 1987 to Nozue

DEPENDENT CLAIMS 9 and 14

If the rejection of independents claims 1 and 12 fall, then dependent claims 9 and 14 are patentable. As such, the rejection of dependent claims 9 and 14 stands or falls with Applicant's independent claim 1.

VIII. CONCLUSION

For the above reasons, Applicant submits that claims 1-11, 12-18 and 24-26 are patentable. It is therefore respectfully requested that

- the rejection of claims 25 and 26 under 35 U.S.C. § 112, first paragraph;
- the rejection of claims 1-7, 10-12, 15-18 and 24 under 35 U.S.C. § 103(a);
- the rejection of dependent claims 8 and 13 under 35 U.S.C. § 103(a); and
- the rejection of dependent claims 9 and 14 under 35 U.S.C. § 103(a);

all be reversed.

Respectfully submitted,
Aaron Reel Bouillett

By _____
Joseph J. Opalach
Registration No.: 36,229
(609) 734-6839

Patent Operations
Thomson Licensing LLC.
P.O. Box 5312
Princeton, New Jersey 08543-5312

August 24, 2007

IX. CLAIMS APPENDIX

1. (Previously presented) An apparatus for determining convergence of an equalizer, comprising:

an equalizer output signal;

a nearest element decision device, the nearest element decision device receiving the equalizer output signal and creating a decision device output signal containing permissible symbol values of a symbol constellation used in transmission of a signal to the apparatus; and

a monitoring circuit, the monitoring circuit receiving the decision device output signal and applying a test criterion to data contained in the decision device output signal so as to determine equalizer convergence.

2. (Previously presented) The apparatus of claim 1, wherein the equalizer is formed to include an infinite impulse response filter.

3. (Previously presented) The apparatus of claim 1, wherein the nearest element decision device is a slicer.

4. (Previously presented) The apparatus of claim 1, wherein the monitoring circuit receives the decision device output signal for a predetermined period of time representing an acquisition of a desired number of transmitted symbol values.

5. (Previously presented) The apparatus of claim 4, further comprising a memory, the memory being coupled to the monitoring circuit and being adapted to store decision device output data and test criteria.

6. (Previously presented) The apparatus of claim 5, wherein the test criteria for determining equalizer convergence includes identifying a desired sample of transmitted symbol values.

7. (Original) The apparatus of claim 6, wherein the desired sample of transmitted symbol values includes at least one of every possible symbol value.

8. (Previously presented) The apparatus of claim 1, wherein the monitoring circuit is coupled to the equalizer, the monitoring circuit resetting the equalizer when the equalizer diverges.

9. (Previously presented) The apparatus of claim 1, wherein the monitoring circuit is coupled to the equalizer, the monitoring circuit resetting the equalizer when the equalizer achieves an invalid state.

10. (Previously presented) The apparatus of claim 1, wherein the equalizer output signal includes an image representative datastream containing data packets.

11. (Previously presented) The apparatus of claim 1, wherein the monitoring circuit is a microprocessor.

12. (Previously presented) An equalizer status monitoring device for use in a digital communication system, the device including an adaptive channel equalizer, a slicer and a monitoring circuit, wherein the digital communications system receives a vestigial sideband modulated signal containing high definition video information represented by a multiple level symbol constellation, the data having a data frame format constituted by a succession of data frames, the adaptive channel equalizer generating a first output signal which is input to the slicer, the slicer generating a second output signal which is input to the monitoring circuit, the second output signal containing permissible symbol values of a symbol constellation used in transmission of a signal in the digital communication system; the monitoring circuit applying a test criteria to the second output signal to determine convergence of the adaptive channel equalizer.

13. (Previously presented) The system of claim 12, wherein the monitoring circuit is coupled to the adaptive channel equalizer and resets the adaptive channel equalizer when the adaptive channel equalizer diverges.

14. (Previously presented) The system of claim 12, wherein the monitoring circuit is coupled to the adaptive channel equalizer and resets the adaptive channel equalizer when the adaptive channel equalizer assumes an invalid state.

15. (Original) The system of claim 12, wherein the test criteria for determining convergence requires identifying at least some transmitted symbol values.

16. (Previously presented) The system of claim 12, wherein the adaptive channel equalizer further comprises an infinite impulse response filter.

17. (Original) The system of claim 12, wherein the test criteria for determining convergence requires identifying at least one of each possible transmitted symbol value.

18. (Previously presented) The system of claim 12 wherein the monitoring circuit is a microprocessor.

19. (Canceled).

20. (Canceled).

21. (Canceled).

22. (Canceled).

23. (Canceled).

24. (Previously presented) A method for use in determining equalizer convergence, the method comprising the steps of:

slicing an equalizer output signal to provide a sequence of symbols, each symbol taken from a constellation of possible transmitted symbols; and

testing at least a plurality of symbols of the sequence to determine if the equalizer is converged or not.

25. (Previously presented) The method of claim 24, wherein the constellation comprises an alphabet of N symbols, where $N > 1$, and the testing step determines that the equalizer is converged if at least M of the N symbols of the alphabet are represented in the plurality of symbols, where $M > 1$.

26. (Previously presented) The method of claim 24, wherein M equals N.

X. EVIDENCE APPENDIX (NONE)

None.

XI. RELATED PROCEEDINGS APPENDIX (NONE)

None.